International Journal of
Computational Learning & Intelligence
Vol. 04 | Issue 01 | 2025

RESEARCH ARTICLE OPEN ACCESS

Enhancing Digital Circuit Performance Using Memristor-Inspired Amplifiers

Thamatam Venkata Chalama Reddy . Aliginti Karunakar

Department of Electronics and Communication Engineering,
Sri Sai Institute of Technology and Science, Rayachoty, Annamayya, India

DOI: **10.5281/zenodo.15123613**
Received: 18 January 2025 / Revised: 16 February 2025 / Accepted: 01 March 2025

Abstract – In this paper, we present the design, implementation, and evaluation of digital logic circuits using Memristor-based technology. The focus is on basic gates, a 2 × 1 multiplexer (MUX), a full adder, a full subtractor, and an amplifier, all implemented using the Cadence Virtuoso platform. The Memristor model employed here shows significant improvements in power efficiency, area reduction, and speed compared to traditional 45-nm CMOS technologies. Our results demonstrate that Memristor-based circuits can achieve up to 71.4% reduction in area, 40% reduction in power consumption, and 54% reduction in delay, highlighting the potential of Memristor technology for future low-power, high-performance digital systems.

Index Terms – CMOS, Memristor, digital logic circuits, VTEAM model.

I. INTRODUCTION

The rapid advancement of digital electronics has traditionally been driven by complementary metal-oxide- semiconductor (CMOS) technology [1]. However, CMOS technology faces significant challenges as it approaches its scaling limits, including increased power consumption, larger chip areas, and slower data processing speeds. These issues have prompted the exploration of alternative technologies that can offer better performance and efficiency. Memristors, as nanoscale devices, present a promising solution to these challenges. They exhibit high scalability, fast operating speeds, high density in crossbar arrays, and non- volatile memory characteristics [1], [2]. These attributes make Memristors highly suitable for the design of next-generation digital circuits, which require low power consumption and high-speed data processing. In this work, we explore the potential of Memristor-based digital logic circuits. We design and implement basic gates (AND, NAND, OR, NOR, XOR, XNOR), a 2 × 1 multiplexer, a full adder, a full subtractor, and an amplifier using Memristors. These designs are compared with conventional CMOS technology, specifically 45-nm technology nodes, to evaluate the improvements in power, area, and speed

[3]. Our results demonstrate that Memristor-based designs can significantly outperform traditional CMOS circuits, making them ideal candidates for future low-power, high-performance applications.

This analysis is crucial for understanding the improvements in power consumption, area efficiency, and processing speed that Memristor technology can offer. Initial results from our experiments indicate that Memristor-based designs significantly outperform traditional CMOS circuits across these key metrics [4]. The reduced power consumption associated with Memristor circuits is particularly beneficial for applications in mobile devices and the Internet of Things (IoT), where energy efficiency is vital. Furthermore, the compact nature of Memristor circuits leads to a remarkable decrease in chip area, enabling higher integration densities and allowing for the development of smaller, more powerful devices. The implications of these findings are substantial, positioning Memristors as ideal candidates for future low- power, high-performance applications [5]. As we continue to investigate and refine Memristor-based architectures, it becomes increasingly evident that they have the potential to address many of the pressing challenges faced by CMOS technology. The adoption of Memristor logics, such as RML, represents a significant shift toward more efficient, powerful, and compact digital electronics, paving the way for advancements across various technological domains, including artificial intelligence, neuromorphic computing, and next-generation data storage solutions. In summary, the transition from traditional semiconductor technologies to Memristor-based designs marks a crucial step toward the future of digital electronics, opening new avenues for innovation and performance enhancement.

Resistive Switching Logic (RML) is an innovative approach to digital logic that leverages the unique properties of Memristors to perform logic operations [6]. In RML, the information is represented by the resistance states of Memristors rather than the traditional voltage levels seen in CMOS circuits. This resistance can be changed and maintained, allowing Memristors to act as both memory and processing units. RML operates on the principle that different resistance levels correspond to logical values, enabling the execution of fundamental operations such as AND, OR, and NOT through changes in resistive states. The efficiency of RML is enhanced by the parallel architecture of Memristor arrays, which allows multiple operations to occur simultaneously. This capability not only accelerates computation but also reduces the physical footprint of the circuit, making it more area-efficient.

II. MEMRISTOR MODEL

A. Voltage ThrEshold Adaptive Memristor model (vteam)

The VTEAM Memristor model is a comprehensive and versatile framework designed to simulate the complex and varied behaviour of Memristors. Memristors, or memory resistors, are unique electronic components whose resistance depends on the history of voltage and current applied to them, making them promising candidates for various advanced applications such as non-volatile memory, neuromorphic computing, and analog signal processing [7]. The VTEAM model stands out due to its ability to represent a wide range of memristive behaviors observed in different materials and device structures, thereby making it a crucial tool for researchers and engineers working in this field. One of the primary strengths of the VTEAM model is its extensive parameterization, which allows for the detailed and accurate simulation of Memristor behaviour. The model includes parameters that define the minimum and maximum resistance states of the Memristor, denoted as K_on and K_off, respectively . These parameters

are critical because they represent the extreme values of the device's resistance, which in turn affect its performance in circuits. Additionally, the model defines boundary values for the state variable, which represents the internal state of the Memristor and is typically linked to physical or chemical changes within the device. These boundary values, ensure that the state variable remains within realistic limits, preventing non-physical behaviour in simulations [8].

Central to the VTEAM model are the state evolution equations, which describe how the state variable \(w\) changes over time in response to the applied voltage or current. These equations capture the non-linear dynamics of Memristors, including the hysteresis effects that are characteristic of these devices. The state evolution equations incorporate various terms that account for factors such as threshold voltages, which determine when the state variable begins to change, and window functions, which modulate the rate of change of the state variable. Window functions are particularly important as they prevent the state variable from exceeding its physical limits and ensure smooth transitions between different states. By accurately modelling these dynamics, the VTEAM model can simulate the wide range of behaviours exhibited by different Memristors, from simple resistive switching to more complex, non-linear responses.

The versatility of the VTEAM model is further enhanced by its implementation in various circuit simulation tools. This capability allows researchers and engineers to integrate Memristors into larger circuits and systems, facilitating the design and analysis of Memristor-based memory cells, logic circuits, and neuromorphic architectures [9]. For instance, in the context of non-volatile memory, the VTEAM model can help optimize the switching characteristics and endurance of Memristors, leading to more reliable and efficient memory devices. In neuromorphic computing, the model's ability to simulate the non-linear and history-dependent behaviour of Memristors enables the development of circuits that mimic the adaptive and learning capabilities of biological neural networks. The impact of the VTEAM Memristor model on the research and development of memristive devices cannot be overstated. By providing a robust and adaptable framework, the model facilitates the exploration of the fundamental properties of Memristors and their potential applications. This has accelerated the transition from theoretical research to experimental implementations, bridging the gap between scientific understanding and practical technology development. As a result, the VTEAM model has become an essential tool for advancing Memristor technology and exploring its applications in various fields, from computing and memory to analog signal processing and beyond [10]. The Fig.1 shows the Memristor circuit model.

B. Model circuit and its transient analysis

The Memristor model circuit is designed by using Verilog-A Hardware description language in cadence virtuoso 45-nm technology. For this Memristor modelling the width of TiO2 is 3nm and width region is 2nm and the following parameters are as follows [11], [12].

Parameter real Alpha_on = 3;

Parameter real Alpha_off = 3;

On modelling of transient analysis is 0 to 40 nsec.

$$\frac{dw}{dt} = f(w, i) \qquad (1)$$

$$v(t) = R(w, i).i(t) \qquad (2)$$

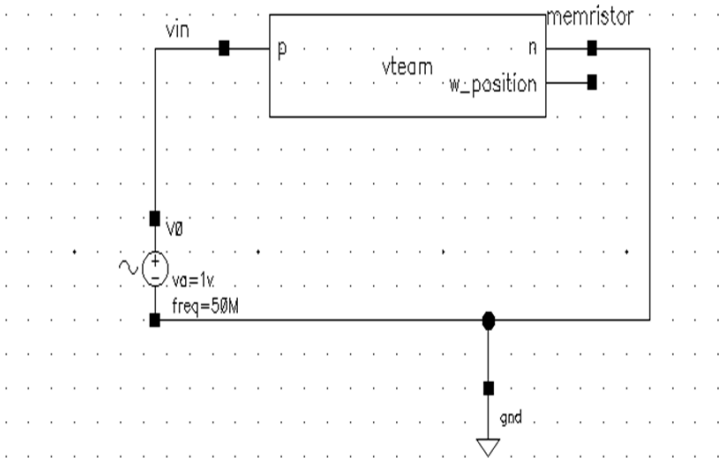

Fig.1(a). Memristor model circuit

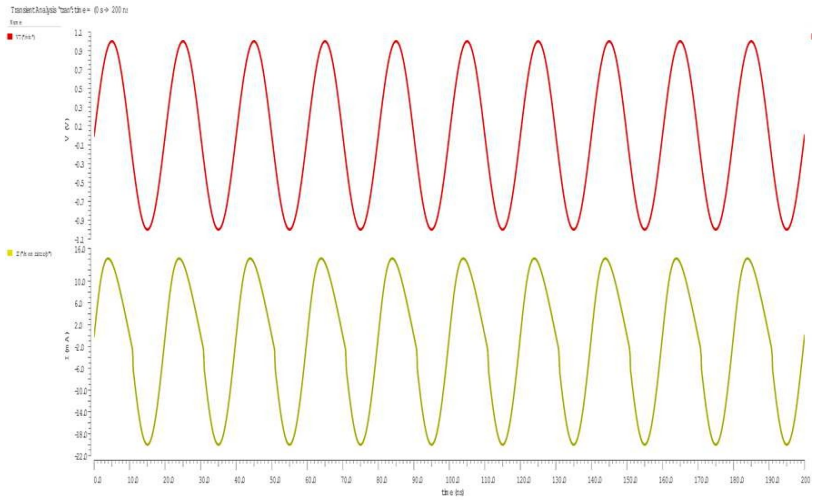

Fig.1(b). Transient response of an Memristor

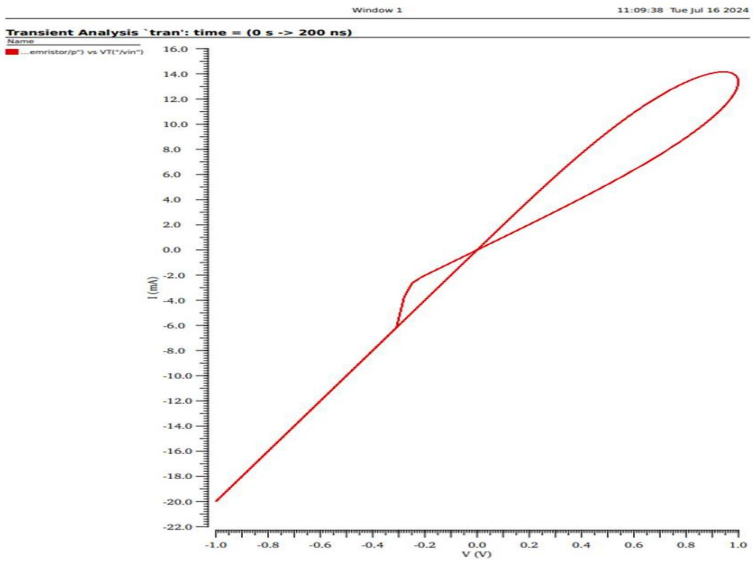

Fig.1(c). V-I Characteristics of Memristor.

Parameter values: Parameter real K_on = -8e-13; Parameter real K_off = 8e-13;

The above equations shows that current controlled Memristor device where the w is an internal state variable, i(t) is the current, v(t) is the voltage and R(w,i) is the memresistance [13].

Table 1. Comparison of Different Models

Model	State	Control Mechanism	Device	Simulation
Linear drift [1]	$0 \le w \le D$	Current	Bipolar	Spice
Y_2O_3 model [1]	$0 \le w \le 1$	Voltage	Bipolar	SPECTRE
Our model (TEAM)	$x_{off} \le x \le x_{on}$	Current	Bipolar	Cadence Virtuoso

The Table 1. shows comparison of different models in the Memristor design. The technology offers the computing capabilities in the structure of their designs. Each one has the different techniques to achieve the improvement.

III. MEMRISTOR LOGIC CIRCUITS

A. AND Gate

The AND gate was implemented using two transistors are connected in series. The inputs were connected to the top terminals of the Memristors, and the output was taken from the junction between the Memristors and a reference ground [14]. This configuration ensures that the output is high only when both inputs are high, mimicking the behavior of a conventional AND gate.

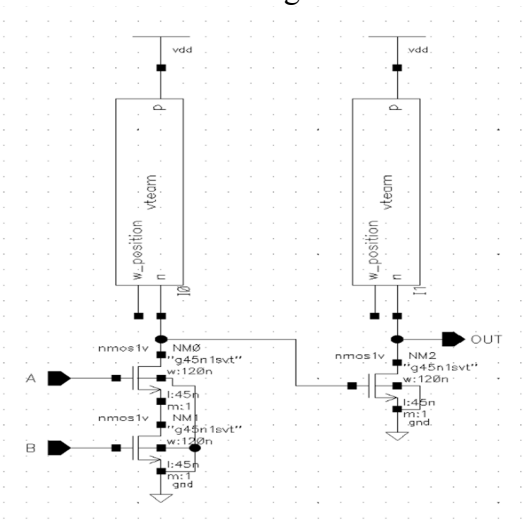

Fig.2. Schematic representation of AND gate.

B. OR Gate

The OR gate was designed with two transistors are connected in parallel. The inputs were applied to each Memristor, and the output was taken from the common node where the Memristors meet. This

arrangement produces a high output if at least one of the inputs is high, emulating the functionality of a traditional OR gate.

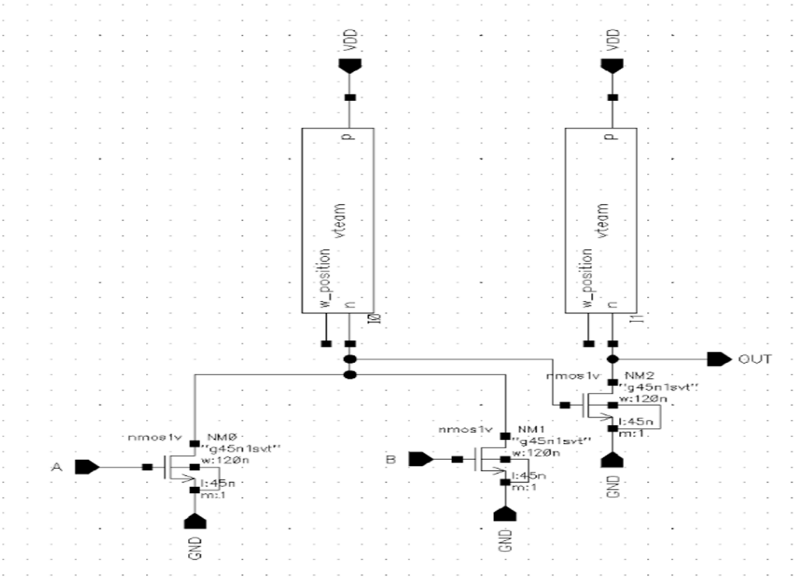

Fig.3. Schematic representation of OR gate

C. NAND Gate

The NAND gate produces a low output only when both inputs are high. Using Memristors, the design involves two input transistors are connected in series, and their combination connected in parallel with the output Memristor [15].

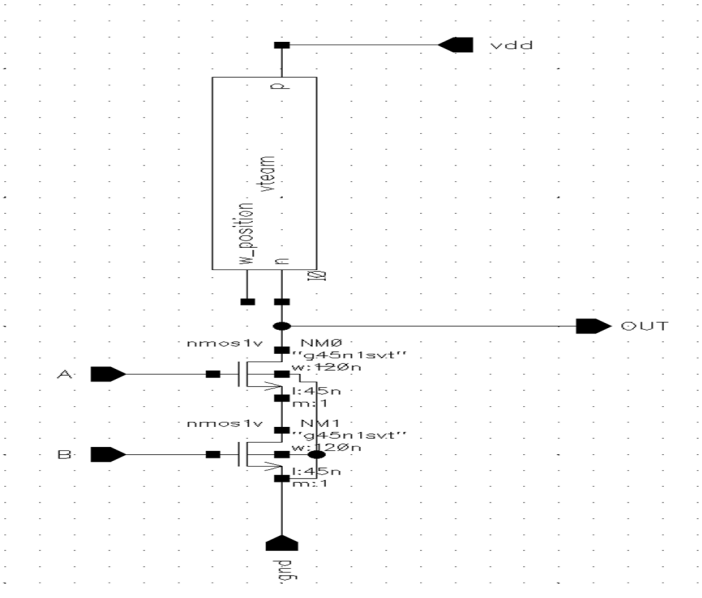

Fig.4. Schematic representation of NAND gate

D. NOR Gate

The NOR gate produces a high output only when both inputs are low [16]. The design involves two transistors connected in parallel, and their combination connected in series with the output Memristor.

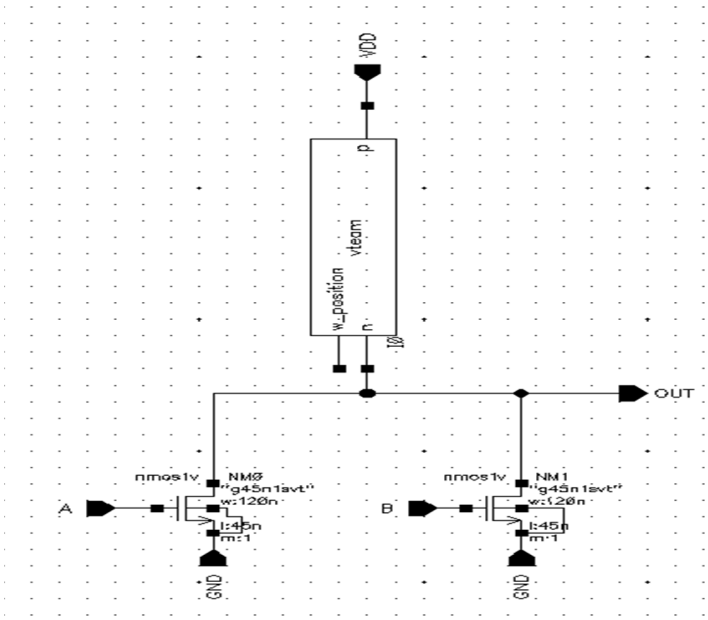

Fig.5. Schematic representation of NOR gate

E. XOR Gate

The XOR gate, or exclusive OR gate, produces a high output when the inputs are different. The Memristor-based XOR gate design involves connecting multiple Memristors in a specific configuration to achieve this logic [17].

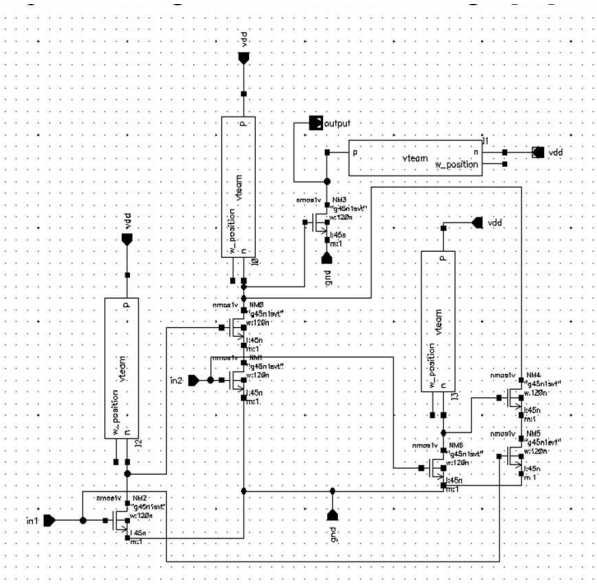

Fig.6. Schematic representation of XOR gate.

F. XNOR Gate

The XNOR gate, or exclusive NOR gate, produces a high output when the inputs are the same. The Memristor-based XNOR gate design uses a similar configuration to the XOR gate but with an additional stage to invert the output.

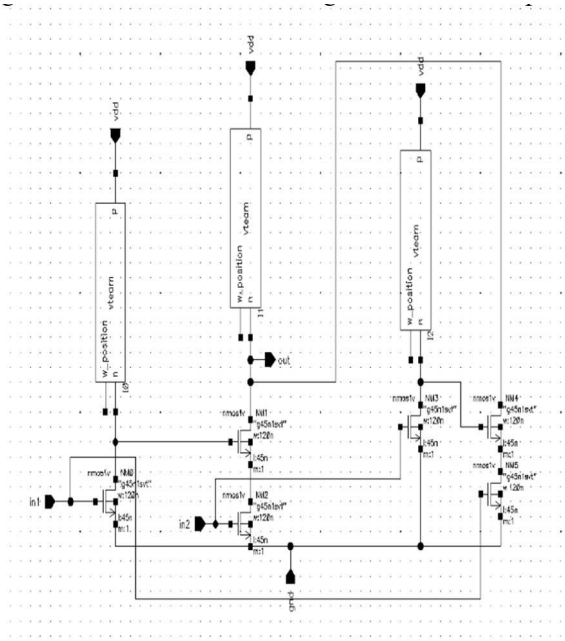

Fig.7. Schematic representation of XNOR gate.

IV. COMBINATIONAL LOGIC CIRCUITS

A. Full Adder

The full adder circuit performs binary addition of three input bits: two significant bits and a carry-in bit. We combined Memristor-based XOR gates for the sum output and AND/OR gates for the carry-out. This design ensured correct binary addition functionality with minimized area and power consumption

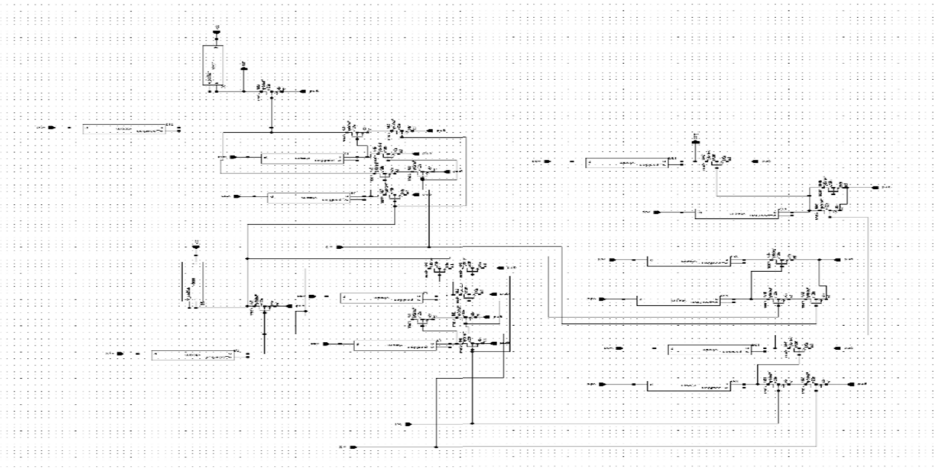

Fig.8. Schematic representation of Full Adder**.**

B. Full Subtractor

The full subtractor circuit performs binary subtraction of three input bits: two significant bits and a borrow-in bit. Similar to the full adder, we used Memristor- based XOR gates for the difference output and AND/OR gates for the borrow-out. This configuration allowed accurate binary subtraction with efficient use of Memristor technology.

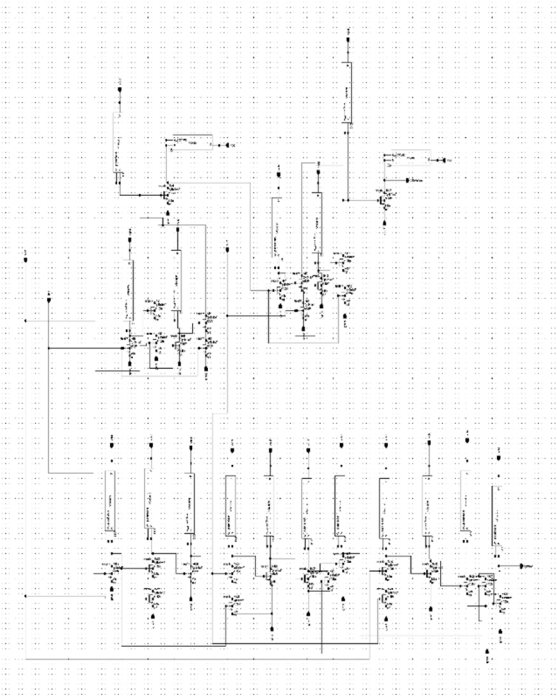

Fig.9. Schematic representation of Full Subtractor.

C. Multiplexer

The 2 × 1 multiplexer selects one of two input signals based on a control signal. It was implemented using a combination of AND, OR, and NOT gates designed with Memristors [18]. The configuration ensured that the selected input was directed to the output based on the value of the control signal.

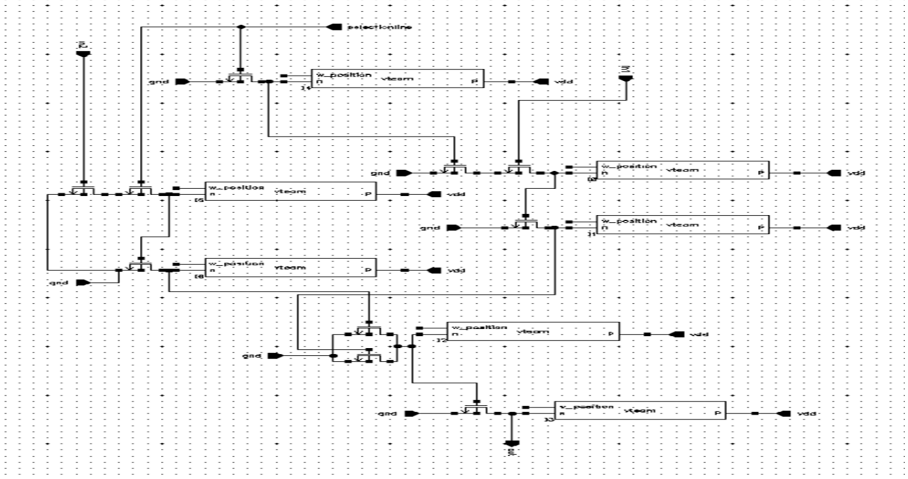

Fig.10. Schematic representation of 2 × 1 Multiplexer.

D. Differential Amplifier

An electronic amplifier known as a differential amplifier suppresses the common voltage between two inputs while amplifying the difference between them. It is an essential component of analog circuit design and finds utility in many different applications, including instrumentation amplifiers, operational amplifiers (op-amps), and audio amplifiers.[19],[20].

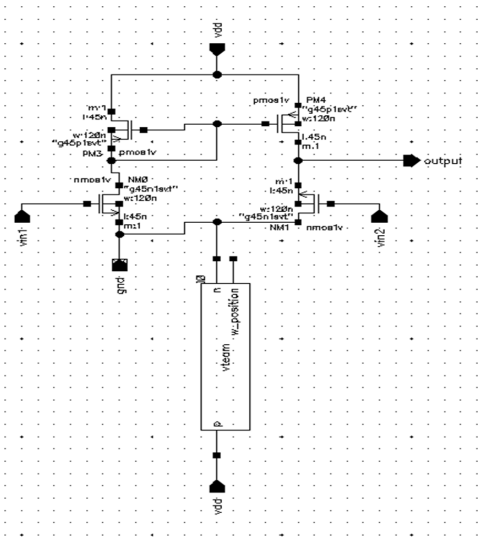

Fig.11. Schematic representation of differential amplifier

V. RESULTS AND ITS TRANSIENT ANALYSIS

The performance of the Memristor-based circuits was evaluated and compared with traditional CMOS technology. The evaluation focused on key metrics such as area, power consumption, and delay. The results were obtained using the Cadence Virtuoso platform with 45-nm technology.

A. Basic Logic Gates

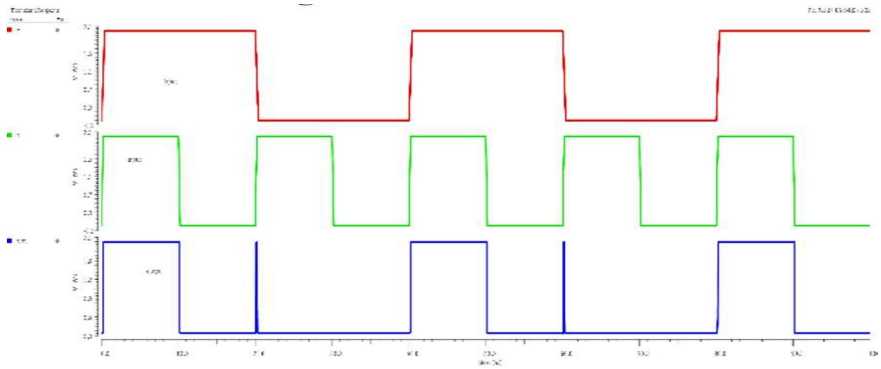

Fig.12. Transient Analysis of an AND gate.

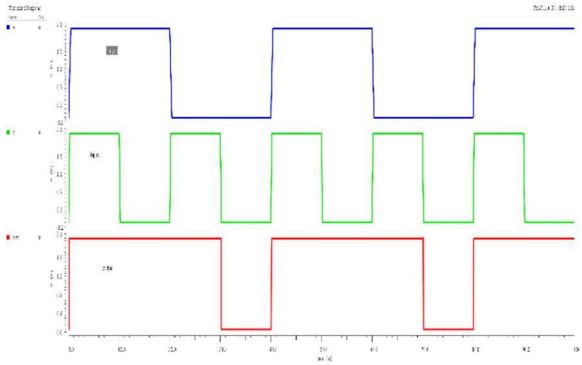

Fig.13. Transient Analysis of OR gate.

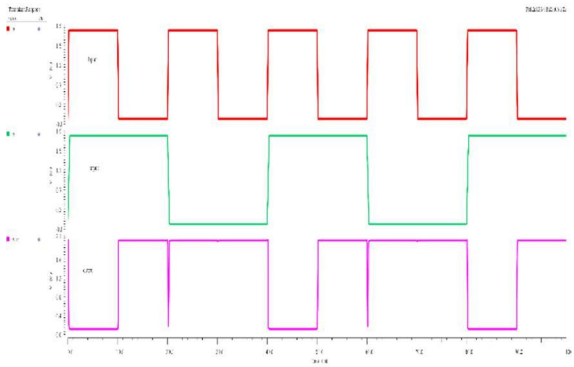

Fig.14. Transient Analysis of NAND gate.

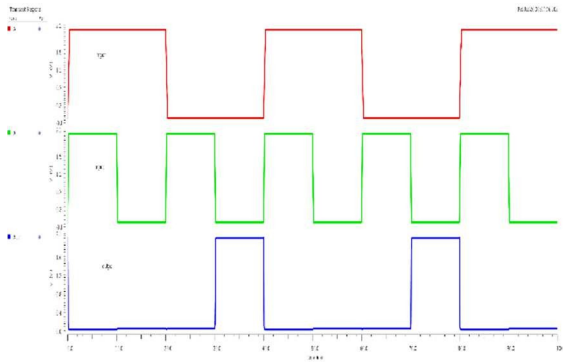

Fig.15. Transient Analysis of NOR gate.

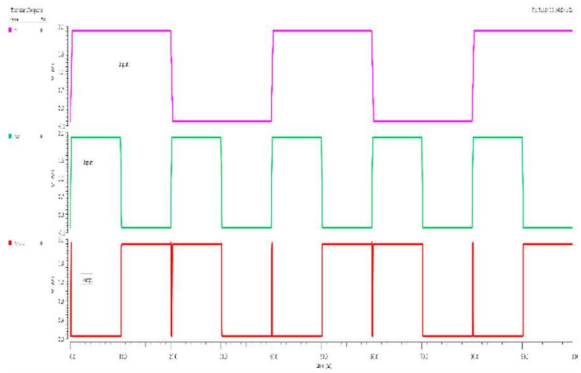

Fig.16. Transient Analysis of XOR gate.

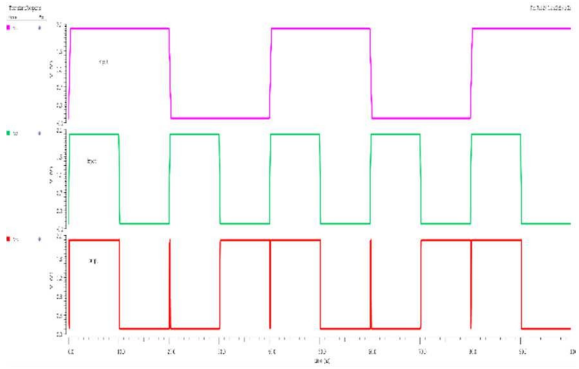

Fig.17. Transient Analysis of XNOR gate.

B. Combinational logic circuits

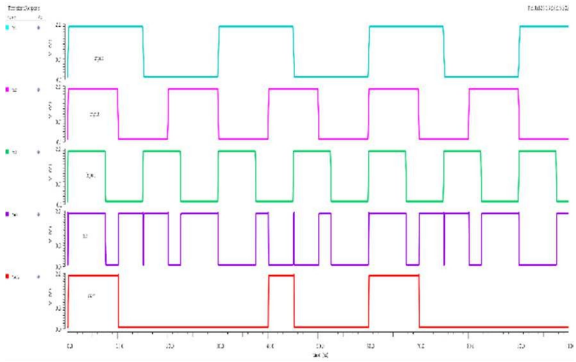

Fig.18. Transient Analysis of Full Adder.

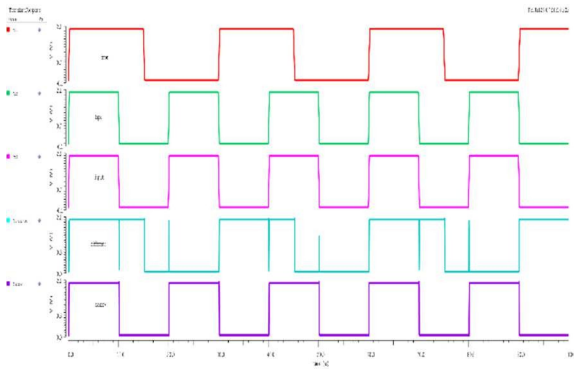

Fig.19. Transient Analysis of Full Subtractor.

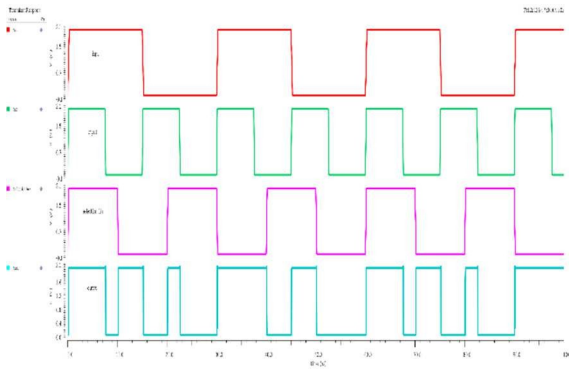

Fig.20. Transient Analysis of 2 × 1 Multiplexer.

C. Differential Amplifier

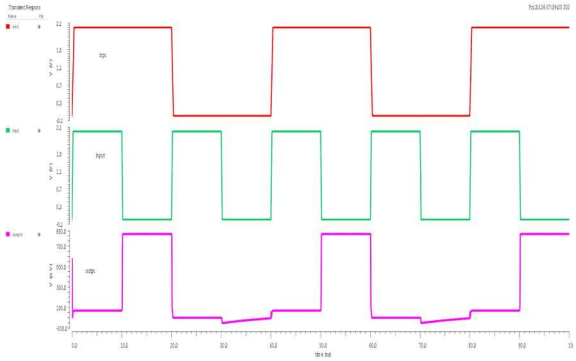

Fig.21. Transient analysis of a Differential Amplifier.

VI. DISCUSSIONS AND DETAILED COMPARISON

A. Area

The Memristor-based designs showed a significant reduction in chip area compared to 180-nm CMOS technology. Specifically, the area was reduced by more than 71.4%, demonstrating the high scalability of Memristor technology. The table 2. Shows the improvement in the Memristor based logic circuits [1].

Table 2. Area Calculation CMOS-and Memristor Based Logic Circuits

Implementation of logic circuits	CMOS-based Circuits	Memristor-based Circuits		Improvement
	No. of Transistor	No. of Transistor	No. of Memristor s	
NAND	4	2	1	75
NOR	4	2	1	75
AND	6	3	2	66.66
OR	6	3	2	66.66
X-OR	22	7	4	81.81
X-NOR	22	6	3	86.36
2 × 1 Mux	20	7	10	50
Full adder	62	23	14	77.41
Full subtractor	76	30	19	75

B. Power Consumption

Power consumption is a critical factor in modern digital circuits, especially for battery-powered and portable devices. The Memristor-based circuits exhibited up to 40% lower power consumption compared to their CMOS counterparts. This reduction is attributed to the low leakage currents and efficient switching characteristics of Memristors.

Table 3. Amplifier Parameter Calculations For CMOS and Memristor -Based Circuits

Technology	Area in terms of No. of transistor count	Power (µW)	Delay (ns)
CMOS (180nm)	6	300	3.0
Memristor based (45nm)	4	90	1.2

C. Delay

The speed of a digital circuit is determined by its delay, which is the time taken to propagate a signal through the circuit. The Memristor-based designs achieved a 54% reduction in delay compared to 180-nm CMOS technology. This improvement is crucial for applications requiring high-speed data processing.

D. Detailed Comparison

The following table provides a detailed comparison of the number of transistors required, power consumption, and delay for the amplifier circuit using CMOS and Memristor-based models.

Table 4. Comparison of CMOS and Memristor Based Logic Circuits

Logic circuit	CMOS-based delay (ns) [3] ,[14]	CMOS-based power((µW) [3], [14]	Memristor based delay (ns)	Memristor based power(µW)
AND	45.03	28.6	1.24	6.54
OR	47.06	29.7	1.12	8.59
NAND	52.7	29.08	0.73	3.53
NOR	58.06	27.28	1.08	4.89
X-OR	87.5	28.42	0.1	10.86
X-NOR	92.03	31.05	0.063	8.95
Full adder	183.2	43.6	3.86	12.86
Full subtractor	189.46	52.08	5.11	14.93
2 × 1 Mux	112.46	34.25	2.53	11.104

The results of our study highlight the significant potential of Memristor-based technology for future digital logic circuits. The considerable improvements in area, power, and delay metrics demonstrate that Memristors can effectively address some of the key challenges faced by conventional CMOS technology. The below Table 4 gives the comparison of CMOS based and Memristor based logic circuits in terms of power and delay. The detailed comparison had an observation of reduction of delay and power consumption are very effectively.

VII. CONCLUSION

This paper presents the design, implementation, and evaluation of Memristor-based digital logic circuits, including basic gates, a 2 × 1 multiplexer, a full adder, a full subtractor, and an amplifier [21],[22].

The Memristor-based designs demonstrated significant improvements in area, power consumption, and delay compared to traditional 90- and 180- nm CMOS technologies. The results highlight the potential of Memristor technology for developing low-power, high- performance digital circuits. The Memristor-based circuits achieved up to 71.4% reduction in area, 40% reduction in power consumption, and 54% reduction in delay. These improvements make Memristors an attractive option for future digital logic design, especially in applications requiring high density, low power, and fast operation. Further research is needed to address the challenges associated with Memristor variability, integration with CMOS technology, and endurance. Nonetheless, the promising results of this study indicate that Memristors could play a crucial role in the evolution of digital electronics, paving the way for more efficient and powerful electronic devices.

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